FREQUENTLY ASKED QUESTIONS

BAA06-40, TRUST for Integrated Circuits

Question: How can I obtain a copy of the BAA06-40 Proposer Information Pamphlet?

Answer: A copy of the Proposer Information Pamphlet can be obtained at http://www.fbo.gov/spg/ODA/DARPA/CMO/BAA06-40/Attachments.html.

Question: When are the White Papers and Full proposals due?

Answer: The white papers are due by 4:00 pm on June 30, 2006 and the full proposals are due by 4:00pm on August 21, 2006.

Question: Are there any classification, International in Traffic Arms Regulation (ITAR), or Export Administration Regulations (EAR) restrictions imposed on this BAA opportunity?

Answer: Please see the following paragraph in Section 1 of the Proposer Information Pamphlet:

"Offerors should submit their research proposals with adequate protection. When research proposals are not classified by other sources, adequate protection can be translated to Company Proprietary (i.e. processing on a closed network, enforced need-to-know, and transmittal by means of Registered Mail). If a question exists regarding classification please contact Darin Smith 703-526-4102 office, 703-807-1779 fax, darin.smith@darpa.mil. In addition, the International Traffic in Arms Regulation (ITAR) may apply and should be considered in your proposal. Additional ITAR information is available at http://www.pmdtc.org/itar_index.htm. If a question exists regarding ITAR please contact SID_International_Security@darpa.mil."

Question: Will a copy of the BAA be posted on www.grants.gov and will you accept submissions through www.grants.gov?

Answer: The BAA will be posted to www.grants.gov however DARPA is not accepting applications through that website at this time. Please submit your white papers and proposals in accordance to the procedures outlined in the Proposer Information Pamphlet.

Question: For the whitepaper coversheet, what do the instructions mean by "Technical Area"?

Answer: The technical areas that are referred to in the instructions on the cover sheet are the technical areas laid out in the Proposer Information Pamphlet. These categories are:

1. Technologies for TRUSTed Integrated Circuits
2. TRUST Against Information Leakage
3. TRUST Against Tamper

4. Metrics and Performance Evaluations of Technologies for TRUST

Question:	Can we include any items or sections that were not addressed in the instructions on the white paper format? If so, will they be included in the six (6) page limit?
Answer:	Yes, you can include items or section that where not address in the white paper format instruction, but they are included in the six (6) page limit on the white papers.

Issues of continuing concern for the TRUST effort involve:

1. Techniques to verify that two chips are identical. These chips could be adjacent chips on a wafer, or two packaged parts. They could be ASIC's or COT's (e.g. FPGA's). The techniques must be applicable to complex chips at the 65nm node or below. The techniques must be applicable to relatively small changes, < 1%, in the number or location of devices on a chip. Ideally, the test(s) will be non-destructive, but at least one of the chips must not be destroyed. It would be desirable if the techniques would scale to comparisons to multiple chips.
2. Unique Identification/Traceability of COTS parts. It is desired to have the capability is to uniquely identify each chip type (ideally each chip) so that counterfeit chips cannot be substituted into supply chain.
3. Unique Identification/Traceability of ASIC's. It is desired to have the capability is to uniquely identify each chip so that counterfeit chips cannot be substituted into supply chain.

Based on requests from several White Paper proposers, the TRUST webpage will offer a feature to facilitate teaming among proposers https://www.davincinetbook.com/teams .